PATENT CLAIMS

1. Method for generating an internal sequence of analog values having a specific period, which corresponds to an external sequence coded in a received signal and is synchronous with it, the external sequence comprising repetitions of a fundamental sequence $(s_1,\ldots,s_N)$ of length N, which substantially corresponds to a sequence of binary values which can be produced by logical combination of a first generating binary sequence $(p_1,\ldots,p_N)$ of length N with a non-constant second generating binary sequence $(q_1,\ldots,q_N)$ of length N, and the first generating binary sequence $(p_1,\ldots,p_N)$ being capable of being generated by a binary feedback shift register of length n, in which a next value (p_i) is produced in each case by binary logical combination of the oldest value (p_{i-n}) with at least one of the values $(p_{i-n+1},\ldots,p_{i-1})$ following it, according to a fixed feedback pattern, and in which no segment of the length n occurs more often than once, so that the position of such a segment is uniquely determined within the fundamental sequence $(s_1,\ldots,s_N)$, **characterized in that** in each case a new input value (a_i) is fed to the input of an analog feedback shift register of length n with a feedback pattern corresponding to that of said binary feedback shift register, which input value is produced by superposition of an analog feedback value derived from the values $(a_{i-n},\ldots,a_{i-1})$ in the analog feedback shift register according to a feedback function with an intermediate value which was produced by a logical combination of the actual value of the external sequence with an actual value (q_i) of the second generating sequence $(q_1,\ldots,q_N)$, the position (i) of which actual value therein follows the position of a

segment in the first generating sequence $(p_1,\ldots,p_N)$, which segment consists of a determinative set of n binary values which were derived from the analog values $(a_{i-n},\ldots,a_{i-1})$ in the analog feedback shift register.

2. Method according to Claim 1, **characterized in that** the first generating sequence $(p_1,\ldots,p_N)$ is an m-sequence of length $N = 2^n-1$, so that each set of n binary values, except for one, occurs exactly once as a segment of length n therein.

3. Method according to Claim 2, **characterized in that** the fundamental sequence is a Gold sequence.

4. Method according to any of Claims 1 to 3, **characterized in that** the actual value (q_i) of the second generating binary sequence $(q_1,\ldots,q_N)$ is in each case read out from a table with the determinative set being used as address.

5. Method according to any of Claims 1 to 4, **characterized in that** the binary sequences each consist of the values +1 and -1 and, apart from possible change of sign, the logical combination is multiplication.

6. Method according to Claim 5, **characterized in that** the magnitude of the feedback function is 1 if the magnitudes of the arguments are each 1.

7. Method according to Claim 5 or 6, **characterized in that** the sign of the feedback function always corresponds to the sign of the combination of the arguments.

8. Method according to any of Claims 5 to 7, **characterized in that** the feedback function is invariant on interchange of the arguments.

9. Method according to any of Claims 5 to 8, **characterized in that** the feedback function is antisymmetric and monotonic as a function of each argument.

10. Method according to any of Claims 5 to 9, **characterized in that** the feedback function is substantially a linear combination of the arguments within substantially each sector characterized by specific values of the signs of the arguments.

11. Method according to Claim 10, **characterized in that** the magnitude of the feedback function substantially corresponds to the mean value of the magnitudes of the arguments.

12. Method according to any of Claims 6 to 11, **characterized in that** the feedback value is produced by multiplication of the value of the feedback function with a factor $k<1$, which is preferably between 0.90 and 0.99.

13. Method according to any of Claims 5 to 12, **characterized in that** the determinative set consists of the binary values which in each case have the same sign as the corresponding analog value $(a_{i-n};\ldots;a_{i-1})$ in the shift register.

14. Method according to any of Claims 1 to 13, **characterized in that** the external sequence corresponds to a plurality of copies, directly in succession with

respect to time, of a basic sequence which is derived from the received signal, the length of which copies corresponds to the length N of the fundamental sequence.

15. Method according to Claim 14, **characterized in that** the basic sequence is generated by adding the values of a plurality of sequences of length N which are derived successively from the received signal.

16. Method according to any of Claims 1 to 15, **characterized in that** a binary output signal indicating complete synchronization is generated if the magnitudes of the values (a_i) of the internal sequence exceed a threshold value.

17. Synchronization circuit for carrying out the method as claimed in any of claims 1 to 16, comprising an input for receiving an external sequence of analog values which is derived from a received signal and an analog feedback shift register (25), a feedback circuit (26) connected thereto with taps according to a specific feedback pattern and intended for evaluating a feedback function for determining a feedback value, and a superposition circuit for superposing the feedback value with an intermediate value, **characterized in that** it additionally comprises a memory (29) from which in each case a value can be read out according to a table with a determinative set derived from the values stored in the analog feedback shift register (25) as address, and a logic element (23) for producing the intermediate value by logical combination of the value read out with the value present at the input.

18. Synchronization circuit according to Claim 17, **characterized in that** a gain block (27) for producing the feedback value from its initial value follows the feedback circuit (26), and the superposition circuit is in the form of an adder (24) for adding the feedback value to the intermediate value.

19. Synchronization circuit according to Claim 17 or 18, **characterized in that** it comprises a discriminator (28) for generating a binary output signal indicating synchronization, the input of which discriminator is connected to the output of the feedback circuit (26) and which discriminator preferably comprises a squaring circuit, a low-pass filter and a threshold value detector.

20. Receiver for receiving a signal, which comprises at least one synchronization circuit according to any of Claims 17 to 19 for deriving an internal sequence from the received signal.

21. Receiver according to Claim 20, **characterized in that** it comprises at least one pair of identical synchronization circuits, one of which is connected via an inverter (20) and the other directly to a common input.

22. Receiver according to Claim 20 or 21, **characterized in that** it comprises at least one pair of identical synchronization circuits which in each case are connected via a sampling element (16; 17) to a common input, with a delay element (18) which shifts the sampled values in each case by a part of a chip length in front of at least one sampling element (17).

23. Receiver according to any of Claims 20 to 22, **characterized in that** it comprises an oscillator (12) for generating a first sinewave signal and a second sinewave signal phase-shifted relative thereto by 90°, and at least one pair of identical synchronization circuits, each with a mixer (11; 13) in front for mixing the received signal with the first sinewave signal or the second sinewave signal.